

## 1 CLAIM LISTING

2  
3 1. (Canceled)

4  
5 2. (Currently amended) A substrate with a via and pad structure  
6 connecting a surface mount component to conductive layers of the substrate,  
7 comprising:  
8 a surface mount component, wherein the surface mount component  
9 includes a package having an upper surface with solderable terminal sides and a  
10 terminal end;  
11 a substrate;  
12 a plated via connected to the conductive layers;  
13 a solder mask surrounding the plated via; and  
14 a conductive pad with a conductive trace connected to the plated via,  
15 wherein the solder mask exposes a part of the conductive pad that extends  
16 beyond the solderable terminal sides of the surface mount component to  
17 increase solder formation between the conductive pad and the solderable  
18 terminal sides and to reduce solder formation at the first plated via ~~The substrate~~  
19 ~~with the via and pad structure of claim 1,~~ wherein the solder mask covers a part  
20 of the conductive pad that extends beyond the solderable terminal end and  
21 reduces solder formation at the terminal end of the surface mount component.

22  
23 3. (Previously presented) The substrate with the via and pad structure  
24 of claim 2, wherein the conductive pad includes a first arm and a second arm that  
25 extend beyond the solderable terminal sides of the surface mount component.

26  
27 4. (Original) The substrate with the via and pad structure of claim 3,  
28 wherein the first arm and the second arm are symmetrically disposed on the  
29 substrate with respect to the plated via.  
30

1           5.     (Original) The substrate with the via and pad structure of claim 2,  
2 wherein the conductive pad includes a first arm, a second arm, and a body.

3  
4           6.     (Original) The substrate with the via and pad structure of claim 5,  
5 wherein the first arm and the second arm are symmetrically disposed on the  
6 substrate with respect to the plated via.

7  
8           7.     (Original) The substrate with the via and pad structure of claim 2,  
9 wherein the conductive pad includes a T-shirt shaped structure.

10  
11          8.     (Original) The substrate with the via and pad structure of claim 7,  
12 wherein the T-shirt shaped structure is symmetrically disposed on the substrate  
13 with respect to the plated via.

14  
15          9.     (Original) The substrate with the via and pad structure of claim 2,  
16 wherein the solder mask is keyhole shaped.

17  
18          10.    (Original) The substrate with the via and pad structure of claim 2,  
19 wherein the solder mask covers the substrate partially or entirely except the  
20 conductive pad and the plated via.

21  
22          11.    (Previously presented) The substrate with the via and pad structure  
23 of claim 2, further comprising solder joint(s), wherein the solder joints have a  
24 greater volume at the solderable terminal sides than at the terminal end of the  
25 surface mount component.

26  
27          12.    (Original) The substrate with the via and pad structure of claim 2,  
28 wherein the substrate is part of a printed circuit board.

29  
30          13.    (Previously presented) The substrate with the via and pad structure  
of claim 2, wherein the substrate is part of a BGA package footprint.

1  
2 14. (Canceled)

3  
4 15. (Currently amended) A substrate with a plurality of via and pad  
5 structures connecting a surface mount component to conductive layers of the  
6 substrate, comprising:

7 a surface mount component, wherein the surface mount component  
8 includes a package having an upper surface with first solderable terminal sides  
9 and a first terminal end and second solderable terminal sides and a second  
10 terminal end;

11 a substrate;

12 a first plated via connected to the conductive layers;

13 a first solder mask surrounding the first plated via;

14 a second plated via connected to an associated conductive layer;

15 a second solder mask surrounding the second plated via;

16 a first conductive pad with a conductive trace connected to the first plated  
17 via, wherein the first conductive pad includes a portion that is exposed to solder  
18 and extends beyond the first solderable terminal sides of the surface mount  
19 component to increase solder formation along the first solderable terminal sides  
20 and to reduce solder formation at the first plated via; and

21 a second conductive pad with a conductive trace connected to the second  
22 plated via, wherein the second conductive pad includes a portion that is exposed  
23 to solder and extends beyond the second solderable terminal sides of the surface  
24 mount component to increase solder formation along the second solderable  
25 terminal sides and to reduce solder formation at the second plated via The  
26 ~~substrate with the plurality of via and pad structures of claim 14, wherein the first~~  
27 ~~solder mask covers and reduces solder formation at the first terminal end of the~~  
28 ~~surface mount component and the second solder mask covers and reduces~~  
29 ~~solder formation at the second terminal end of the surface mount component.~~  
30

1        16.    (Previously presented) The substrate with the plurality of via and pad  
2 structures of claim 15, wherein each of the first and second conductive pads  
3 include a first arm and a second arm.

4  
5        17.    (Original) The substrate with the plurality of via and pad structures of  
6 claim 16, wherein each of the first and second conductive pads is symmetric to  
7 the first plated via and the second plated vias, respectively.

8  
9        18.    (Original) The substrate with the plurality of via and pad structures  
10 of claim 15, wherein the first and second conductive pads include a first arm, a  
11 second arm, and a body.

12  
13       19.    (Original) The substrate with the plurality of via and pad structures of  
14 claim 18, wherein each of the first and second conductive pads is symmetric to  
15 the first plated via and the second plated vias, respectively.

16  
17       20.    (Original) The substrate with the plurality of via and pad structures of  
18 claim 15, wherein each of the first and second conductive pads include a T-shirt  
19 shaped structure.

20  
21       21.    (Original) The substrate with the plurality of via and pad structures of  
22 claim 20, wherein each of the T-shirt shaped structures is symmetric to the first  
23 and second plated vias, respectively.

24  
25       22.    (Original) The substrate with the plurality of via and pad structures of  
26 claim 15, wherein each of the first and second solder masks is a ring surrounding  
27 the first and second plated vias, respectively.

28  
29       23.    (Original) The substrate with the plurality of via and pad structures of  
30 claim 15, wherein each of the first and second solder masks is a keyhole shape  
and surrounds the first and second plated vias, respectively.

1        24. (Original) The substrate with the plurality of via and pad structures of  
2 claim 15, wherein each of the first and second solder masks cover the substrate  
3 partially or entirely except the first and second conductive pads and the first and  
4 second plated vias.

5  
6        25. (Previously presented) The substrate with the plurality of via and  
7 pad structures of claim 15, further comprising solder joint(s), wherein the solder  
8 joint(s) have a greater volume at each of the solderable terminal sides than at  
9 each terminal end of the surface mount component.

10  
11       26. (Previously presented) The substrate with the plurality of via and  
12 pad structures of claim 15, wherein the separation along the substrate between  
13 the first and second solder masks defines the length of the surface mount  
14 component to be soldered.

15  
16       27. (Original) The substrate with the plurality of via and pad structures of  
17 claim 15, wherein the substrate is part of a printed circuit board.

18  
19       28. (Previously presented) The substrate with the plurality of via and pad  
20 structures of claim 15, wherein the substrate is part of a BGA package footprint.

21  
22       29. (Original) The substrate with the via and pad structure of claim 2,  
23 wherein solder mask is a ring surrounding the plated via.

24       30. (Canceled)

25  
26       31. (Canceled)

27  
28       32. (Canceled)

1        **33. (Canceled)**

2

3        **34. (Currently amended) The substrate with the plurality of via and pad**  
4 **structures of claim 14, wherein the first conductive pad extends beyond the**  
5 **terminal side of the component a maximum distance that reduces solder wicking**  
6 **without generating electrical shorts between the first conductive pad and an**  
7 **adjacent plated via.**

8

9        **35. (Canceled)**

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

30